Electrical reliability aspects of HfO₂ high-κ gate dielectrics with TaN metal gate electrodes under constant voltage stress

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Received 17 August 2004; received in revised form 1 February 2005
Available online 31 March 2005

Abstract

The dielectric breakdown property of ultrathin 2.5 and 5.0 nm hafnium oxide (HfO₂) gate dielectric layers with metal nitride (TaN) gate electrodes for metal oxide semiconductor (MOS) structure has been investigated. Reliability studies were performed with constant voltage stressing to verify the processing condition effects (film thicknesses and post metal annealing temperatures) on times to breakdown. The leakage current characteristics are improved with post metal annealing temperatures (PMA) for both 2.5 and 5.0 nm HfO₂ physical thicknesses. However, it is more prominent (~2 orders of magnitudes) for 2.5 nm HfO₂ film thickness. The values of oxide-trapped charge density and interface-state density are also improved for 2.5 nm HfO₂ film. The different stages of charge-trapping behaviors, i.e., stress-induced leakage current, soft and hard breakdown mechanisms have been detected. During constant voltage stress of the MOS capacitors, an increase in the time-dependent gate current is observed, followed by the occurrence of several fluctuations. The amplitude of the fluctuations is much larger in the 5.0 nm HfO₂ gate dielectric layer compared to the 2.5 nm HfO₂ layer. After the occurrence of such fluctuations, the current–voltage characteristics exhibited an increased in gate current compared to the fresh (unstressed) devices.

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1. Introduction

In order to scale CMOS devices to smaller dimensions (65 nm) while maintaining good control of the short-channel effects and good sub-threshold behavior, the gate oxide thickness of MOSFET devices must be reduced in approximate proportion to decrease in the channel length [1]. The typical leakage current of SiO₂ at a gate bias of 1 V, changes from 10⁻¹² A/cm² at 3.5 nm to 10 A/cm² at 1.5 nm due to quantum-mechanical tunneling [2]. Due to the high leakage currents, increased power consumption, intrinsic device reliability, and circuit instabilities associated with SiO₂ of this thickness, a high-permittivity (high-κ) gate dielectric (e.g., Si₃N₄, HfSi₁ₓO₁₋ₓ, HfO₂, ZrO₂) with a low leakage current and at least equivalent capacitance, performance, and reliability will be required [3,4]. In addition to thermodynamic stability on Si, other key parameters related to HfO₂ gate dielectrics are: large band gap with more than 1 eV tunneling barrier for both electron and hole carriers (conduction and valence band offsets) in order to have low leakage currents and low interface trap defect densities. However, the transition from SiO₂ to HfO₂ does have some obstacles that need to be overcome. One of the potential problems with HfO₂ is to figure out a good interface with underlying
substrate [5,6]. Process integration issues must be solved and reliability must be assured before any new material or processing technique can be used in a process line. Recently, Onishi et al. [7] demonstrated that a high temperature post metal anneal (PMA) prior to metallization improved channel carrier mobility as well as the sub-threshold slope of HfO2.

The advantages of metal gate electrode over poly-Si gates are much lower gate resistance, desirable work function setting, no gate depletion effect, etc. Tantalum nitride (TaN) is one of the most promising for NMOS gate electrode applications because of the combination of low work function, excellent diffusion barrier properties, and high melting point [8]. TaN and tungsten nitride (WN) have been found to block the diffusion of oxygen better than titanium nitride (TiN). Also, TaN is a hard material, chemically inert, corrosion resistant, and has good shock and heat-resistant properties [9].

High-\(k\) gate dielectrics are known to be “trap-rich” materials [10]. During high field tunnel injection of electrons into the oxide layer, microscopic defects like neutral electron traps, charge trapping, and interface states are generated in the dielectric/semiconductor system [11]. The neutral electron traps generated during high field stress can act as a stepping stone for the injected electron at a low voltage, giving rise to a stress-induced leakage current (SILC). The term neutral trap does not mean that the traps have to be neutral. It is used to signify the traps that lead to breakdown are not necessarily associated with a positive or negative charge [12]. The neutral traps can capture a hole to become positively charged or capture an electron to become negatively charged. During stress, the density of neutral electron traps increases, which leads to a gradual increase in SILC. The gate leakage current increase at low field is probably due to the trap-assisted tunneling process through the neutral traps generated in HfO2 by analogy to the SILC in SiO2 [11]. A conductive path is created in the gate oxide layer after reaching a critical trap density, which results in a soft breakdown (SBD) or quasi-breakdown [10]. Then, the Joule heating in the local conductive path leads to lateral propagation of the leakage spots and the oxide is finally broken down, signified as a hard breakdown (HBD) [13]. So, the SILC phenomenon is the total of trap assisted tunneling (TAT) currents on the whole gate area, while breakdown phenomena take place very locally through a conduction path in the oxide layer. In the case of SILC, the traps act both as coulombic scattering centers, and as pathways for increased the local leakage currents [12]. For the SBD characteristic, the electron tunneling from the TaN gate to the Si-substrate takes place via multiple traps in a very localized area (in HfO2 layer) of the MOS capacitor [14]. In this paper, the work is focused on the electrical characterization to study the effect of post metallization annealing and constant voltage stressing for reliability of ultra-thin HfO2 gate dielectrics with TaN metal gate electrode.

2. Experimental

Two sets of HfO2 films covering the dielectric thicknesses 2.5 and 5.0 nm were fabricated using the atomic layer deposition process on p-type Si wafers. After that, a \(~\sim\)90-nm thick TaN gate electrode (resistivity 50–60 \(\mu\)\(\Omega\) cm) was deposited in a 100 W RF reactive sputtering deposition unit with a Ta target in N2/Ar mixture (N2 = 50%) for 30 s and then a 90 min 100 W RF Ta reactive sputtering in N2/Ar mixture (N2 = 5%) at 5 mTorr operating pressure through a shadow mask. Post metallization annealing (PMA) for TaN gate electrodes was applied in a N2 ambient for 10 s using a high-temperature substrate heater (base pressure: 10\(^{-8}\) Torr, operating pressure: 50 Torr) at temperatures of 600 and 800 \(^\circ\)C, respectively. The post metal thermal annealing in N2 prior to the final forming gas annealing is a common practice for physical vapor deposited nitride gates, since the sputter-deposited nitride films are not dense enough. For a good ohmic contact for the MOS capacitor, a 3000 Å thick aluminum (Al) film was deposited on the backside of the Si wafer using the DC sputtering technique. Finally, forming gas annealing was done in a H2/N2 (1:9) ambient at 400 \(^\circ\)C for 30 min in a tube furnace.

The capacitance voltage (\(C-V\)), current voltage (\(I-V\)) characteristics and constant voltage stressing (CVS) of the MOS capacitors were studied using Agilent 4284A and Agilent 4155C parameter analyzers. The SILC measurement can be assessed by applying a constant voltage stress for a definite period of time and determining the change in leakage current repeatedly. The low-level leakage currents and the stress-generated oxide trap densities were measured before and after different stress levels on the various oxide thicknesses. During those measurements on thin gate oxide of MOS structures, such phenomena as SILC, SBD, and HBD had been observed.

3. Results and discussion

The measured gate leakage current density as a function of the applied bias at different post metal annealing conditions for TaN/HfO2 (2.5 nm)/Si and TaN/HfO2 (5.0 nm)/Si samples are shown in Fig. 1(a) and (b), respectively. The leakage currents are compared in the accumulation region for n-MOS (on p-type substrate, electron injection from gate) as a function of applied gate voltage. It is observed that the current density is reduced after the post-metallization anneal in N2 ambient. This indicates that the PMA treatment is efficient in reducing the density of bulk traps or dangling bonds.
present in the HfO$_2$ layer. Table 1 compares the values of leakage current density measured at $\pm 1$ V applied gate voltage of two different dielectric thicknesses with different post metal annealing conditions. It can be noticed that after 800 °C PMA in N$_2$ ambient for 10 s, the leakage current is improved by almost three orders of magnitude in case of 2.5 nm physical dielectric thickness of HfO$_2$ layer, but in case of 5 nm physical dielectric thickness the improvement of leakage current after PMA is not too much. This phenomenon may be possible due to the following reasons: (a) the trapping probability is likely increased for thicker HfO$_2$ layer. Some traps may be participating in the leakage current [15]. (b) During high-temperature PMA, the interfacial layers’ thicknesses (both at metal–dielectric and dielectric–substrate) increase with temperature [16]. It was observed from the high-resolution transmission electron microscopy (HRTEM) images [17] that the thicknesses of the interfacial layers are enhanced after the N$_2$ annealing for 800 °C, e.g., 0.6 nm before annealing and 1.8–2.2 nm after annealing at the dielectric–substrate interface. For the thinner HfO$_2$ sample (2.5-nm thick) the interface layer might affect the leakage current much more than that of the thicker HfO$_2$ (5-nm thick) sample. According to the published papers, the interfacial layer formed between HfO$_2$ and Si may be SiO$_2$ [18] or HfSi$_x$O$_y$ [19]. For this paper, a distinct interface layer was observed by HRTEM. However, it was difficult to determine from electron energy loss spectroscopy (EELS) and energy dispersive X-ray spectroscopy (EDX) whether this interface layer was composed of SiO$_2$ or HfSi$_x$O$_y$ (c) Also from, XRD results (not shown here) showed that 2.5 nm HfO$_2$ sample was still amorphous after the same annealing condition. However 5 nm HfO$_2$ sample became partially crystallized after 800 °C PMA, which may be responsible for the different leakage current behavior after 800 °C PMA between 2.5 and 5 nm HfO$_2$ samples. So, the crystallization temperature of the thin film is depending on deposition methods as well as thickness of the film. Lee et al. [20] reported that the crystallization temperature of HfO$_2$ was 700 °C. Conley et al. [21] showed that for 5.1-nm thick HfO$_2$ film the crystallization occurred at 850 °C. In addition, Tewg et al. [22] reported that under the same annealing condition, the 10-nm thick film has a higher crystallization temperature than the 100-nm thick films.

Generally, two types of traps are associated with the leakage current of the oxide layer: interface-trapped charge and oxide-trapped charge. The interface-trapped

![Fig. 1](image_url)

**Table 1**

The values of leakage current density measured at $\pm 1$ V, the fixed oxide charge density, the interface-state density for as-deposited and PMA TaN/HfO$_2$/Si samples

<table>
<thead>
<tr>
<th>Processing conditions</th>
<th>Gate current density at $\pm 1$ V (A/cm$^2$)</th>
<th>Oxide trapped charge ($Q_{ot}$) (cm$^{-2}$)</th>
<th>Interface-state density ($D_{it}$) (eV$^{-1}$cm$^{-2}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>TaN/HfO$_2$ (2.5 nm)/Si</td>
<td>TaN/HfO$_2$ (5.0 nm)/Si</td>
<td>TaN/HfO$_2$ (2.5 nm)/Si TaN/HfO$_2$ (5.0 nm)/Si</td>
</tr>
<tr>
<td>As deposited</td>
<td>$4.7 \times 10^{-5}$</td>
<td>$6.9 \times 10^{-8}$</td>
<td>$2.85 \times 10^{-12}$ $1.22 \times 10^{12}$</td>
</tr>
<tr>
<td>PMA at 600 °C</td>
<td>$4.84 \times 10^{-6}$</td>
<td>$1.64 \times 10^{-8}$</td>
<td>$1.10 \times 10^{-12}$ $1.87 \times 10^{12}$</td>
</tr>
<tr>
<td>PMA at 800 °C</td>
<td>$5.52 \times 10^{-8}$</td>
<td>$1.11 \times 10^{-8}$</td>
<td>$1.21 \times 10^{-12}$ $1.37 \times 10^{12}$</td>
</tr>
</tbody>
</table>
charges originate from defects such as structural defects related to the deposition process, metallic impurities or bond-breaking process at the insulator–substrate interface. However, oxide-trapped charges is associated with defects in the HfO2, was found to depend mostly on the injecting electrode. In fact, positive charges is found for gate injection that can be attributed to an anode hole injection process in the HfO2 layer [15].

The interface-trapped charge density \(D_{it}\) at midgap (from Hill’s method) [23] and the oxide-trapped charge density \(Q_{ot}\) using capacitance–voltage \((C-V)\) and conductance–voltage \((G-V)\) techniques for both 2.5 and 5 nm HfO2 thicknesses with different PMA conditions, were determined from the following equations:

\[
D_{it} = \frac{(2/qA)[G_{\text{max}}/\omega]}{[(G_{\text{max}}/\omega \cdot C_{\text{acc}})^2 + (1 - C_{\text{in}}/C_{\text{acc}})^2]} \tag{1}
\]

and

\[
Q_{ot} = C_{\text{acc}} \Delta V_{fb} \tag{2}
\]

where \(G_{\text{max}}\) is the maximum conductance in the \(G-V\) plot with its corresponding capacitance \(C_m\) and \(C_{\text{acc}}\) is the accumulation capacitance. \(\Delta V_{fb}\) is the flat-band voltage shift measured using double voltage sweep i.e., from inversion to accumulation and back to inversion. \(A\) is the area of the capacitor, \(q\) is the electronic charge and \(\omega\) is the angular frequency applied during the measurement. From Table 1, it can be noticed that the values of \(Q_{ot}\) and \(D_{it}\) are improved in case of 2.5 nm HfO2 films with PMA, which is consistent with the decrease in leakage current. However, for 5 nm HfO2 films both the \(Q_{ot}\) and \(D_{it}\) values are not changed too much with PMA conditions, and the same phenomena are observed in leakage current measurement too (see from Table 1).

When voltages are applied to an MOS capacitor, the oxide suffers from several degradation mechanisms. CVS measurements were carried out to determine the gate oxide reliability of the MOS capacitors. All samples were stressed in the accumulation regime, which implies a minimum voltage drop over the substrate and excludes gate depletion effects [24]. Initially HfO2 has in-grown traps that may play an important role in dielectric wear-out [10]. As time progresses, applied voltage generates traps in the oxide [25]. These traps act both as coulombic scattering centers and as pathways for increased, local leakage currents, usually called SILC [26]. The traps that are generated during a high voltage stress are charged negatively near the cathode and positively near the anode due to electrons tunneling into and out of the traps [25]. The measured total current density \(J_{\text{mea}}\) at any time \(t'\) and at a fixed voltage is a sum of three different components:

\[
J_{\text{mea}} = J_{\text{tun}} + J_{\text{leak}}(0) + J_{\text{SILC}}(t) \tag{3}
\]

where, \(J_{\text{tun}}\) is the tunneling current in an ideal oxide having no traps. \(J_{\text{leak}}(0)\) is the leakage current due to neutral electron traps that exist in fabricated devices and \(J_{\text{SILC}}(t)\) is the SILC contribution. Some researchers have proposed that SILC is caused by interface-state generation [27], while others claim that it is due to bulk-oxide electron-trap generation [28]. Still others have proposed that it is due to non-uniformities or weak spot formations in the oxide films [29].

SILC can be measured from the difference of the pre-stress gate current \([J_g(\text{fresh})]\) and post-stress gate current \([J_g(\text{stress})]\), i.e.,

\[
\text{SILC} = [J_g(\text{stress})] - [J_g(\text{fresh})] \tag{4}
\]

Stress induced leakage current density versus applied bias characteristics for 800 °C PMA in \(N_2\) ambient of TaN/HfO2 (5 nm)/Si structure before and after constant voltage stressing (−3.0 V) for different stressing time (120, 180 and 240 s) is shown in Fig. 2. It is observed that the magnitude of gate leakage current is increased with increasing the applied stressing time, which signifies that the larger stressing time generates more neutral traps, and more electrons tunnel from cathode to traps and traps to anode inside the oxide. SILC is composed of two components: a transient component and a DC component [30]. The transient component consists of trap filling, as electrons tunnel from cathode into traps too distant from the anode for efficient tunneling to the anode. The trap-assisted tunneling through the oxide causes the DC component.

A popular method of measuring the neutral trap density buildup is to measure the SILC, which is widely accepted due to trap-assisted tunneling [11,31]. Xie et al. [32] proposed a first-order kinetic model to analyze the defect instabilities in ultra-thin oxides. According to this model, the reasonable assumption is that the defect creation probability is exponentially dependent on the

![Fig. 2. SILC measurements of TaN/HfO2/Si (800 °C PMA treatment) under −3.0 V constant voltage stressing for 120, 180 and 240 s.](image)
depth of the defect precursor in the oxide, implying that tunneling is an important aspect of the defect-creation mechanism. During constant voltage stress of dielectrics, a change in gate current is observed. In this work, the initial (low injection) part of the gate current during CVS (to be discussed later in Fig. 4) is approximately linear. This linear part of the SILC growth curve is used as the rate of trap creation in the oxide under stress, same as reported by Buchanan et al. [33] for SiO2 gate dielectric. However, the increase in gate current is not saturating with stressing time. So, the charge-trapping behavior itself cannot completely explain the increase in gate current.

The change in gate current during stressing is modeled by taking into account the density of positive charge build-up and the charged traps due to stressing. To interpret the experimental results quantitatively, consider \( 0 \) be the density of traps/volume in the oxide that can capture an electron with probability \( P_n \). Capture of an electron generates an immobile charged center that causes the high leakage current in the dielectric. Because electron capture determines the immobile charged center generation kinetics, the emission probability of an electron is zero after the immobile charged center generation goes to zero. Following the charged center kinetics, it can be written as [34]

\[
\frac{dQ_o(t)}{dt} = -P_n [Q_o(0) - Q_o(t)]Q_e \tag{5}
\]

where the quantity \([Q_o(0) - Q_o(t)]\) is the instantaneous density of traps available for electron capture after stressing time \( t \). \( Q_e \) is the average injected electron density. The solution of Eq. (5), with the boundary conditions \( Q_o(t) = 0 \) when \( t = 0 \) and \( Q_o(t) = Q_o(0) \) when \( t = \infty \), is

\[
Q_o(t) = Q_o(0) \left[ 1 - \exp\left( -\frac{t}{\tau} \right) \right] \tag{6}
\]

where \( Q_o(t) \) is the gate current observed during stressing and \( Q_o(0) \) is the optimum value of \( Q_o(t) \). \( \tau \) is the time constant and is given by

\[
\tau = \frac{1}{(P_n Q_e)} = \frac{1}{(\sigma \sigma Q_e)} = \frac{q}{\sigma J_g} \tag{7}
\]

where \( \sigma \) is the mean thermal velocity of electron in HfO2 and is approximately equal to the electron drift velocity. \( J_g \) is the mean current density injected into the gate dielectric during the electrical stress, which is approximately proportional to \( Q_o \). \( q \) is the electronic charge (\( \sim 1.6 \times 10^{-19} \) C) and \( \sigma \) is the electrons trap cross-section and can be defined as the ratio of the capture probability to the thermal velocity of the electron.

Eq. (6) can be re-written

\[
\log \left( 1 - \frac{Q_o(t)}{Q_o(0)} \right) = -\frac{t}{\tau} \tag{8}
\]

The experimental plot of \( \log(1 - \{Q_o(t)/Q_o(0)\}) \) versus \( t \) for TaN/HfO2 (5 nm)/Si sample with PMA at 800 °C in N2 ambient is used to extract the values of \( \tau \) for different constant voltage stressing at \( -2.5 \), \(-3\), \(-3.5 \) and \(-4 \) V, which is not shown here. Now considering Eq. (6), the time constant \( \tau \) as a function of the inverse of \( J_g \) injected into the gate insulator during constant voltage stressing at different constant voltages is plotted in Fig. 3. The solid line is a linear fit to the data of this experimental plot. From the slope of this linear fit, the value of \( \sigma \) is easily obtained and it is \( 1.52 \times 10^{-17} \) cm². The radius of the trap cross-section is 0.011 nm.

Therefore, the change in gate leakage current density during stressing \([\Delta J(t) = J(t) - J(0)]\) is modeled by taking into account the positive build-up of charges. The time-dependent gate current density \([\Delta J(t, V_g)]\) can be expressed as [35]:

\[
\Delta J(t, V_g) = A[1 - \exp(-t/\tau)] + \beta(V_g)^d \tag{9}
\]

The first term of Eq. (9) accounts for the building up of charges in the gate dielectric with a time constant \( \tau \), considering Eq. (6). The second term of Eq. (9) takes into account the SILC contribution to the gate current, which increases with time according to a power law with an exponent \( d \) and the voltage dependent trap generation rate \( \beta \). The value of \( \sigma \), found in the high-k gate dielectrics \( (1.52 \times 10^{-17} \) cm² for HfO2) is small compared to \( 1.5 \times 10^{-10} \) cm² in SiO2. The obtained \( \sigma \) value is consistent with that reported by Houssa and co-workers [36], i.e., \( 1.5 \times 10^{-17} \) cm². These small values for the trap cross section suggest that the traps generated during the electrical stress are neutral central in HfO2 layer [11]. The increase in gate leakage current observed in Fig. 4 during CVS (at \(-3.0 \) V) as a function of stress time for PMA at 800 °C of TaN/HfO2 (5.0 nm)/Si samples can be expressed by Eq. (9). The lines (marked as Trapping and SILC) in Fig. 4 have been fitted to the data.

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Fig. 3. Diagram illustrating \( 1/J_g \). Data for this curve are taken from the plot (not shown) of \( \log(1 - [Q_o(t)/Q_o(0)]) \) as a function \( t \) with different CVS at \(-2.5\), \(-3\), \(-3.5 \) and \(-4 \) V.
considering only the buildup of charges (or, charge trapping) in the HfO$_2$ (5.0 nm) layer and the SILC contribution individually. Here the experimental results are quite well reproduced when both charge trapping and the SILC contributions are included.

The time evolution of the gate current for different HfO$_2$ gate dielectric thicknesses with TaN gate electrodes (Un-annealed, PMA at 600 °C and PMA at 800 °C temperatures in N$_2$ ambient) are shown in Fig. 5(a) and (b) during constant voltage stress at −2.0 V and −3.5 V, respectively. During stress experiments, the breakdown is detected as an abrupt decrease of oxide resistance and it is considered as SBD or HBD as shown in Fig. 5(a) and (b) depending on the magnitude of the event. The stress currents show an initial jump and then gradually increase with some fluctuations and eventually reach hard breakdown. From Fig. 5(a) and (b), it can be noticed that the leakage current is improved and time-to-breakdown during CVS for both SBD and HBD increase with increasing PMA temperatures, where as, in case of TaN/HfO$_2$ (~2.5 nm)/Si 600 °C PMA sample, the breakdown mechanism (both SBD and HBD) happen earlier compare to un-annealed sample. The degradation of the oxide during stress results from the formation of a localized percolation path between the gate electrode (TaN) and the substrate (p-Si). A critical number of traps are generated in the gate dielectric layer and at the interface, which in turn form percolative clusters. During stress if the damage is small, the percolation path is narrow, the conduction properties corresponds to SBD but when the damage is significant, the initial defect path is much wider, the post-breakdown situation corresponds to HBD. Fluctuation of the leakage current in the soft breakdown region results from the trapping–detraping of electrons in the percolation clusters. But, the radius of the soft breakdown path of HfO$_2$ layer or the origin of soft breakdown may be different since high-$k$ dielectrics are in general bi-layer structures (an interface and a bulk HfO$_2$ layer [10]).

Fig. 6(a) and (b) shows the pre- and post-stress leakage current ($I$–$V$) characteristics in which all the modes of stress-induced features can be observed: SILC, SBD and HBD for un-annealed and 800 °C post metal annealed TaN/HfO$_2$ (2.5 nm)/Si samples, respectively. During the oxide degradation after constant voltage stress (stage 1), the well-known SILC is observed. The CVS is applied further to the samples and leakage currents are measured again. When the fluctuation mode starts, the gate current suddenly jumps; an anomalous increase of the SILC is observed which is shown in Fig. 6(a) and (b) (stage 2). Soft breakdown consists of an oxide breakdown without the strong thermal effects that lead to an irreversible failure of the device. The electron traps are created in these ultra-thin HfO$_2$ oxide layers during the high field injection of electrons and that they are an important precursor effect for the oxide breakdown. The fluctuation mode should be regarded as an oxide failure even though the oxide does

Fig. 4. The time dependence of the current density increase observed during constant voltage stressing at −3.0 V of 800 °C post metal annealed TaN/5.0 nm HfO$_2$/Si MOS structure. Solid lines and dashed lines are fits using Eq. (9).

Fig. 5. (a) Breakdown characteristics of TaN/HfO$_2$ (2.5 nm)/Si MOS structures during constant voltage stress −2.0 V. (b) Breakdown characteristics of TaN/HfO$_2$ (5.0 nm)/Si MOS structures during constant voltage stress −3.5 V.
not have a destructive breakdown. The last stage (stage 3) of the oxide is the total destruction of the capacitor structure. This is seen in Fig. 6 (a) and (b) as the dramatic increase of the leakage current. Multiple soft breakdowns are observed in Fig. 6 (b) where the evolution of the gate voltage during the CVS is shown. Comparing the Fig. 6(a) and (b), the higher annealing temperature results in lower remaining trap density (and thus lower SILC), similar results are also observed from Table 1. To confirm the mechanisms of SBD and HBD are different in terms of Weibull slope, experiments are in process to characterize and analyze the statistical properties of the SBD and HBD of the samples.

4. Conclusion

Electrical characteristics of MOS capacitors with ALD deposited HfO₂ gate dielectric and TaN gate electrodes have been reported. After 800 °C PMA in N₂ ambient for 10 s, the leakage current is improved with 2.5 nm physical dielectric thickness of HfO₂ layer, where as for 5 nm layers the improvement of leakage current after PMA is not significant. The values of both \( Q_{ot} \) and \( D_{it} \) are decreased with PMA in 2.5 nm HfO₂ gate dielectrics, however both are moderately increased for 5 nm HfO₂ gate dielectrics. The increase of the gate current density observed during the gate voltage stress are not saturating with stressing time. The charge-trapping behavior itself cannot completely explain the increase in gate current. Here the experimental results are quite well reproduced when both charge trapping and the SILC contributions are included. The leakage current is improved and time-to-breakdown during CVS for both SBD and HBD increase with increasing PMA temperatures, except in case of TaN/HfO₂ (~2.5 nm)/Si 600 °C PMA sample, the breakdown mechanism (both SBD and HBD) happen earlier compare to un-annealed sample. So, the electrical reliability characteristics investigated here suggest that the integration of TaN gate electrodes with HfO₂ films can be suitable for MOS device applications with enhanced process optimization.

Acknowledgement

This research is partially supported by NSF project DMI-0300032.

References


